CMOS FULLY DIFFERENTIAL 4TH ORDER OTA-C LOWPASS FILTER

NAME: NASSER OSMAN

ECE 510 – CMOS MIXED-SIGNAL IC DESIGN

PROFESSOR: DR. CHIANG

DATE: MARCH 19TH, 2009.

SPICE MOS Model Statements for CMOS Technology

(based on 0.25μm technology)

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.MODEL tsmc25N NMOS (                LEVEL=11 &
VERSION=3.1      TNOM=27       TOX=5.8E-9  &
XJ=1E-7      NCH=2.3549E17   VTH0=0.4308936  &
K1=0.3519429   K2=0.0298493   K3=1E-3 &
K3B=0.0592323   W0=1E-5      NLX=1.465901E-7  &
DVT0W=0       DVT1W=0       DVT2W=0  &
DVT0=0.0183405   DVT1=4.897584E-3 DVT2=-0.0252658  &
U0=455.3033362  UA=5.223592E-10  UB=1.104713E-18  &
UC=3.287888E-11  VSAT=1.050993E5   A0=1.2318623  &
AGS=0.3043334   B0=6.67749E-8 B1=5E-6     &
KETA=8.518046E-4   A1=0       A2=1  &
RDSW=509.5675851   PRWG=0.0227558   PRWB=-1E-3  &
WR=1 WINT=2.126497E-9 LINT=4.393474E-9 & XL=-3E-
8 XW=0 DWG=-3.409033E-9  &
DWB=2.794842E-9  VOFF=-0.1026054   NFACTOR=0.1344887  &
CIT=0       CDSC=1.527511E-3  CDSCD=0  &
CDSCB=0       ETA0=3.48737E-3   ETAB=4.557986E-4  &
DSUB=3.045473E-3   PCLM=1.0446257   PDIBLC1=0.1441952  &
PDIBLC2=4.513382E-4  PDIBLCB=-2.816756E-5  DROUT=0.4698725  &
PSCBE1=1.761109E10   PSCBE2=3.772916E-9 PVAG=0.0361824  &
DELTA=0.01      MOBMOD=1       PRT=0  &
UTE=-1.5      KT1=-0.11     KT1L=0  &
KT2=0.022     UA1=4.31E-9    UB1=-7.61E-18  &
UC1=-5.6E-11    AT=3.3E4     WL=0  &
WLN=1       WW=0       WWN=1  &
WWL=0       LL=0       LLN=1  &
LW=0       LWN=1       LWL=0  &
CAPMOD=2       XPART=0.4      CGDO=6.27E-10  &
CGSO=6.27E-10    CGBO=0       CJ=1.918655E-3  &
PB=0.9784049   MJ=0.4721729   CJSW=4.441595E-10  &
PBSW=0.9419636   MJSW=0.2871118   PVTH0=1.342985E-3  &
PRDSW=-61.8357222  PK2=-3.140724E-3  WKETA=7.512693E-4  &
LKETA=-6.144062E-3  )



.MODEL tsmc25P PMOS (LEVEL=11 & VERSION=3.1            TNOM=27
TOX=5.8E-9 &
XJ=1E-7           NCH=4.1589E17      VTH0=-0.6158735 &
K1=0.4598379      K2=0.0399415       K3=0 &
K3B=8.7410723      W0=1E-6           NLX=1E-9 &
DVT0W=0              DVT1W=0             DVT2W=0 &
DVT0=0.6249485      DVT1=0.203296       DVT2=-0.0513763 &
U0=158.67524      UA=2.200024E-10   UB=4.457415E-18 &
UC=1.02138E-10    VSAT=1.85064E5      A0=1.3826397 &
AGS=0.4192977      B0=2.844099E-6    B1=5E-6 &
KETA=0.0208695      A1=0              A2=1 &
RDSW=968.5463       PRWG=-0.1026483     PRWB=-0.325 &
WR=1              WINT=2.748811E-8    LINT=8.71907E-9 &
XL=-3E-8          XW=0              DWG=-4.087585E-8 &
DWB=2.032008E-8     VOFF=-0.15          NFACTOR=1.5460516 &
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```

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PDIBLC2=1.204519E-3    PDIBLCB=2.37525E-3    DROUT=0 &
PSCBE1=3.011456E10    PSCBE2=3.037042E-7    PVAG=8.9564294 &
DELTA=0.01            MOBMOD=1              PRT=0 &
UTE=-1.5             KT1=-0.11            KT1L=0 &
KT2=0.022            UA1=4.31E-9          UB1=-7.61E-18 &
UC1=-5.6E-11         AT=3.3E4            WL=0 &
WLN=1                WW=0                WWN=1 &
WWL=0                LL=0                LLN=1 &
LW=0                LWN=1               LWL=0 &
CAPMOD=2               XPART=0.4            CGDO=5.59E-10 &
CGSO=5.59E-10        CGBO=0               CJ=1.882857E-3 &
PB=0.9891317        MJ=0.4679789       CJSW=3.67186E-10 &
PBSW=0.9884654       MJSW=0.3562128       PVTH0=3.923756E-3 &

[illegible]
LKETA=-0.0232426      LVSAT=1.257E5          )
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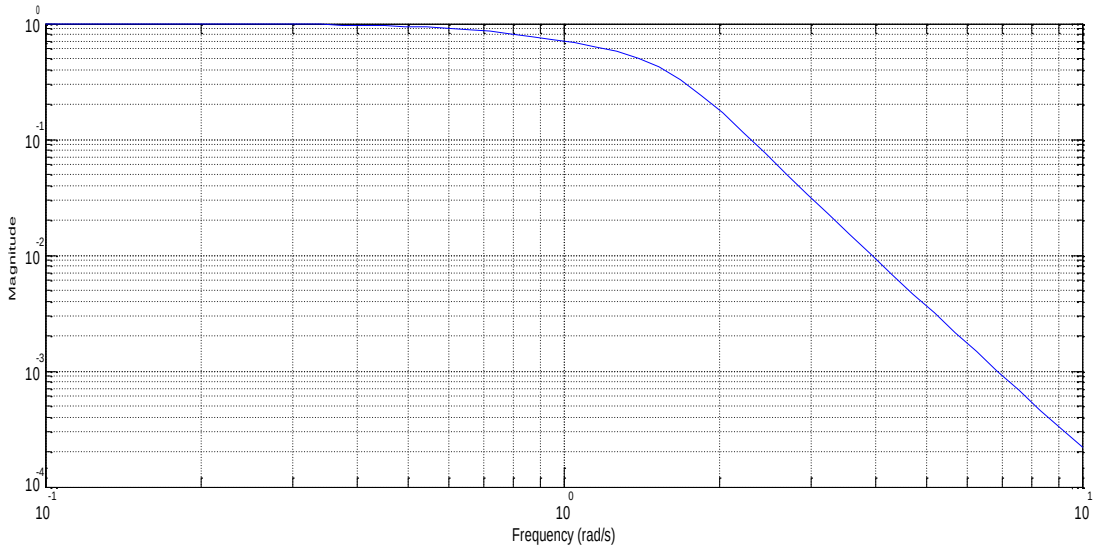
OVERVIEW

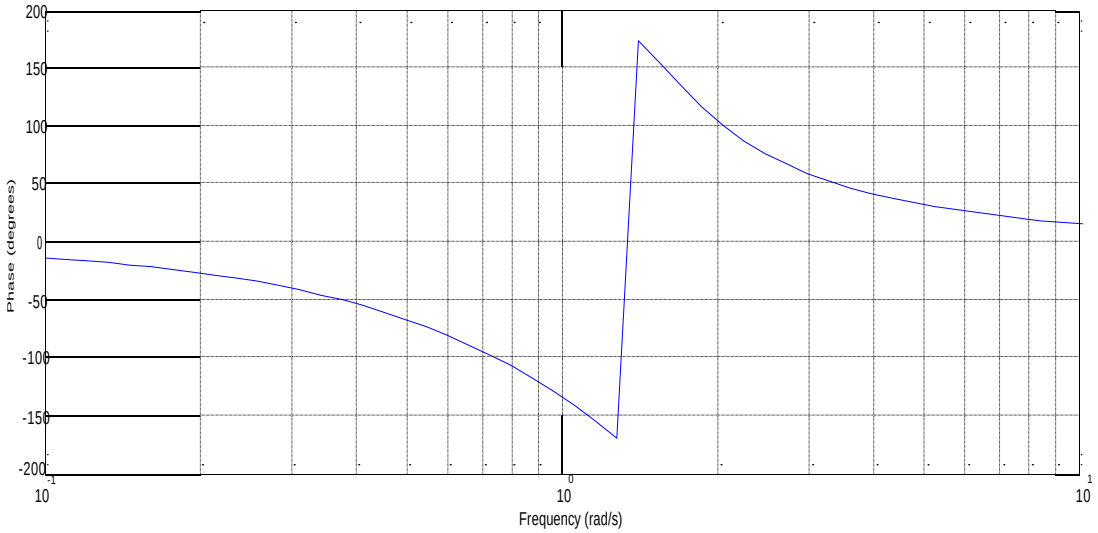
There are three main technologies utilized in the design of high-frequency integrated continuous-time (CT) filters, gm-C based, Mosfet-C based, and RLC-gm-based, gm-C which is well suited for the MHz range and the latter of which is used in the GHz spectrum range. Therefore, based on the given specs namely cut-off frequency, gm-C based would be the best candidate for this project.

The goal of this project was to accurately model and simulate a linear 4^{th} order fully differential low-pass OTA-C filter with a tunable cut-off frequency range of 7MHz-15MHz (11MHz nominal). OTA is an acronym for Operational Transconductance Amplifier. In simplistic terms, an OTA is an Op Amp ‘minus’ its low-impedance output buffer. Nowadays, integrated circuits are implemented as fully differential circuits. The reason for this is because fully differential circuits offer SNR benefit, better noise immunity, and reject common-mode interference. For this project, the folded-cascode OTA was selected to implement the respective gm-cells.

DESIGN APPROACH

The first phase in the design process was to verify and analyze the system's transfer function by simulating it in MATLAB which produced the following frequency response.





Once the system transfer function was analyzed, the next phase in the design process was to select an appropriate OTA topology to model the specified transfer function. Multiple feedback OTA have passband sensitivity better than cascade, additionally an arbitrary transfer function may be realized using this topology. Based on the given spec namely a provided transfer function, the multiple-loop feedback OTA topology seemed like a good candidate in order to meet design specs. This was followed by a derivation of the transfer function of the topology to obtain Vout/Vin in terms of the capacitances.

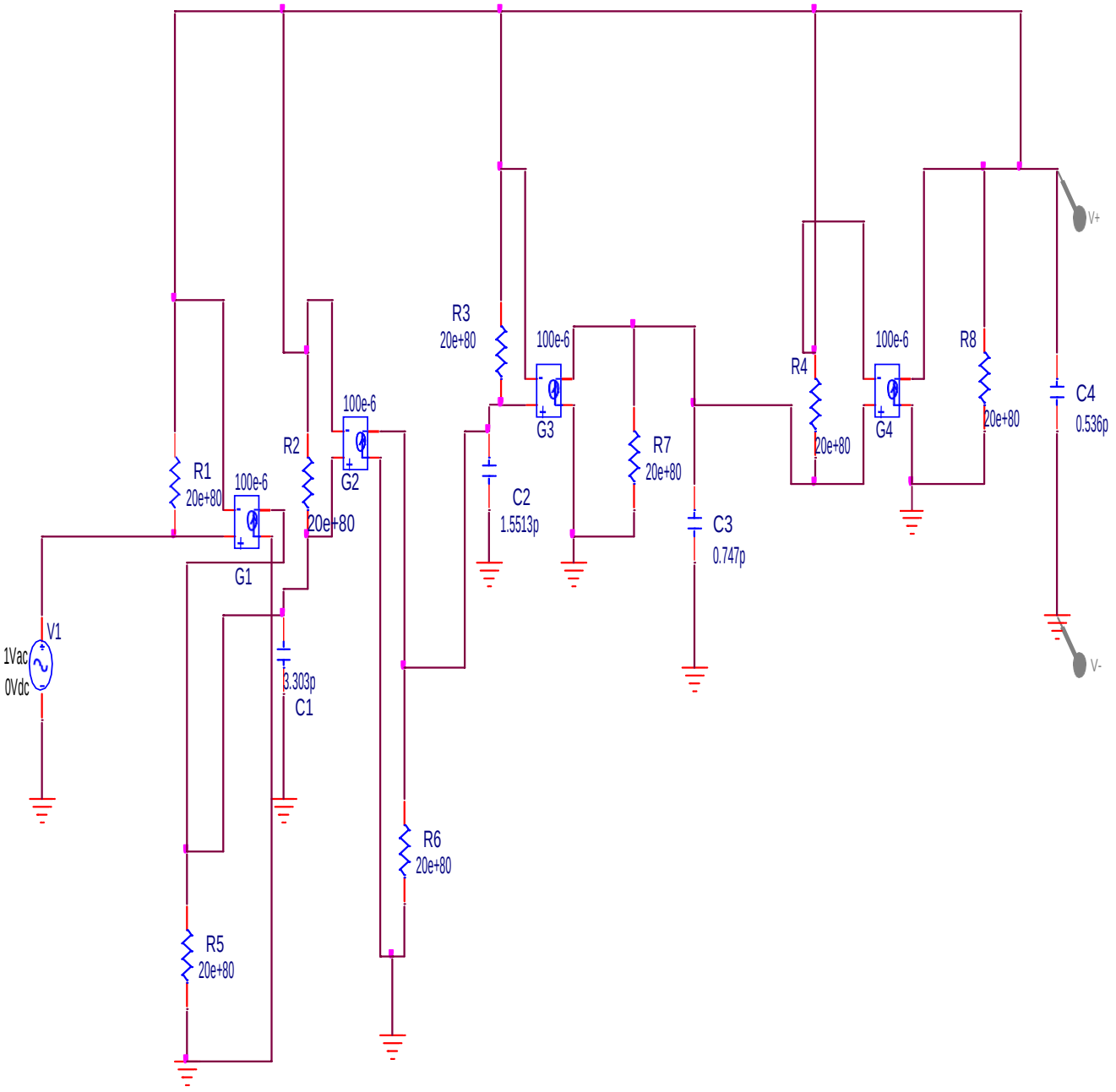
The next phase in the design process was to accurately model the gm-cell device utilizing CMOS (feature size 25um). Initially, the current sources were modeled using ideal current sources. The folded-cascode OTA was selected to implement the gm-cell based on its high input and high output impedance, producing reasonable transconductance gain suitable for this project.

The following phase of the design process involved testing the gm-cell by way of achieving a 1^{st} order low-pass filter response with a specified cut-off frequency.

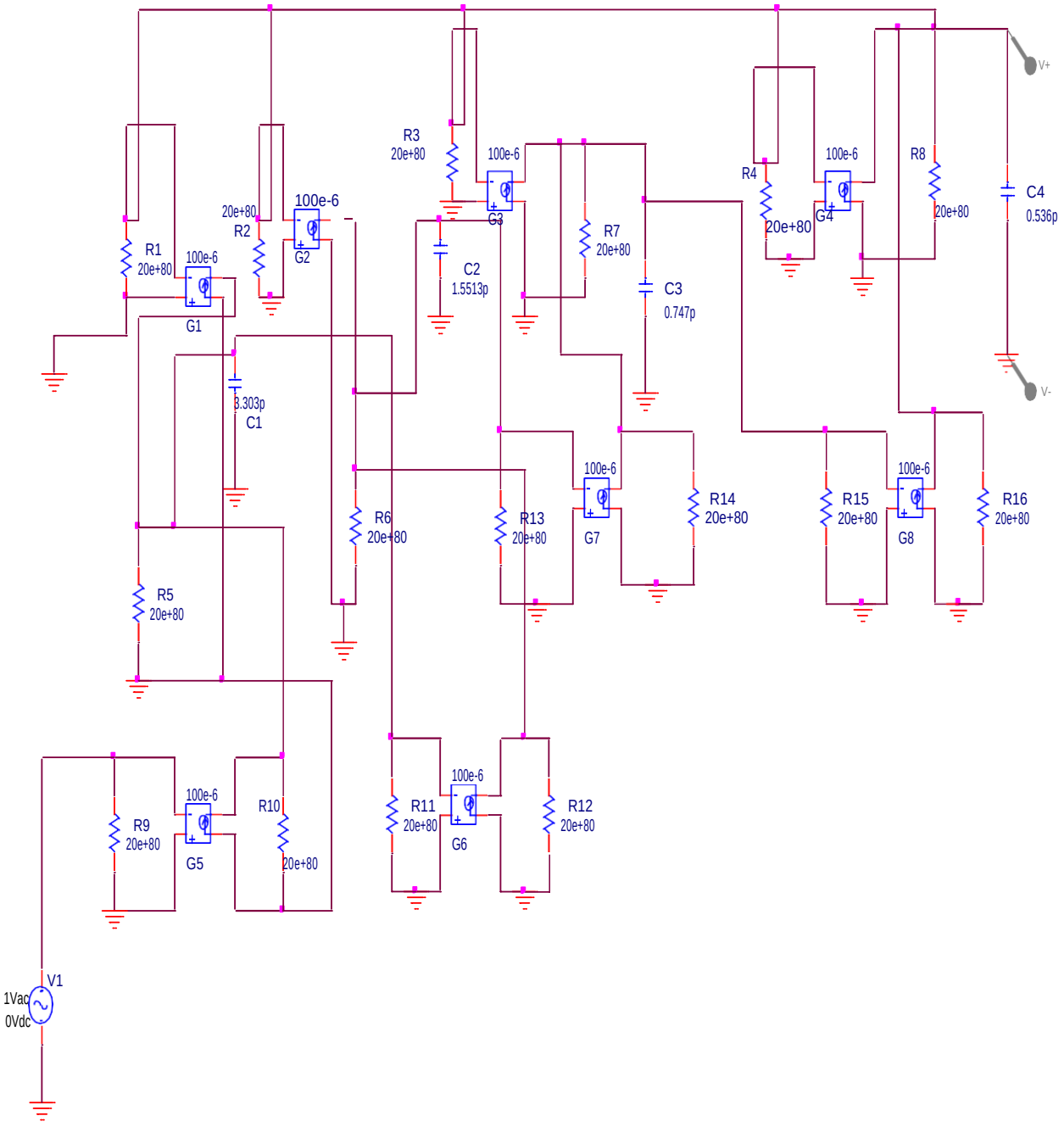
Finally, the independent OTAs were interconnected to produce a final working 4^{th} order OTA-C low-pass OTA filter.

SPICE CIRCUITRY

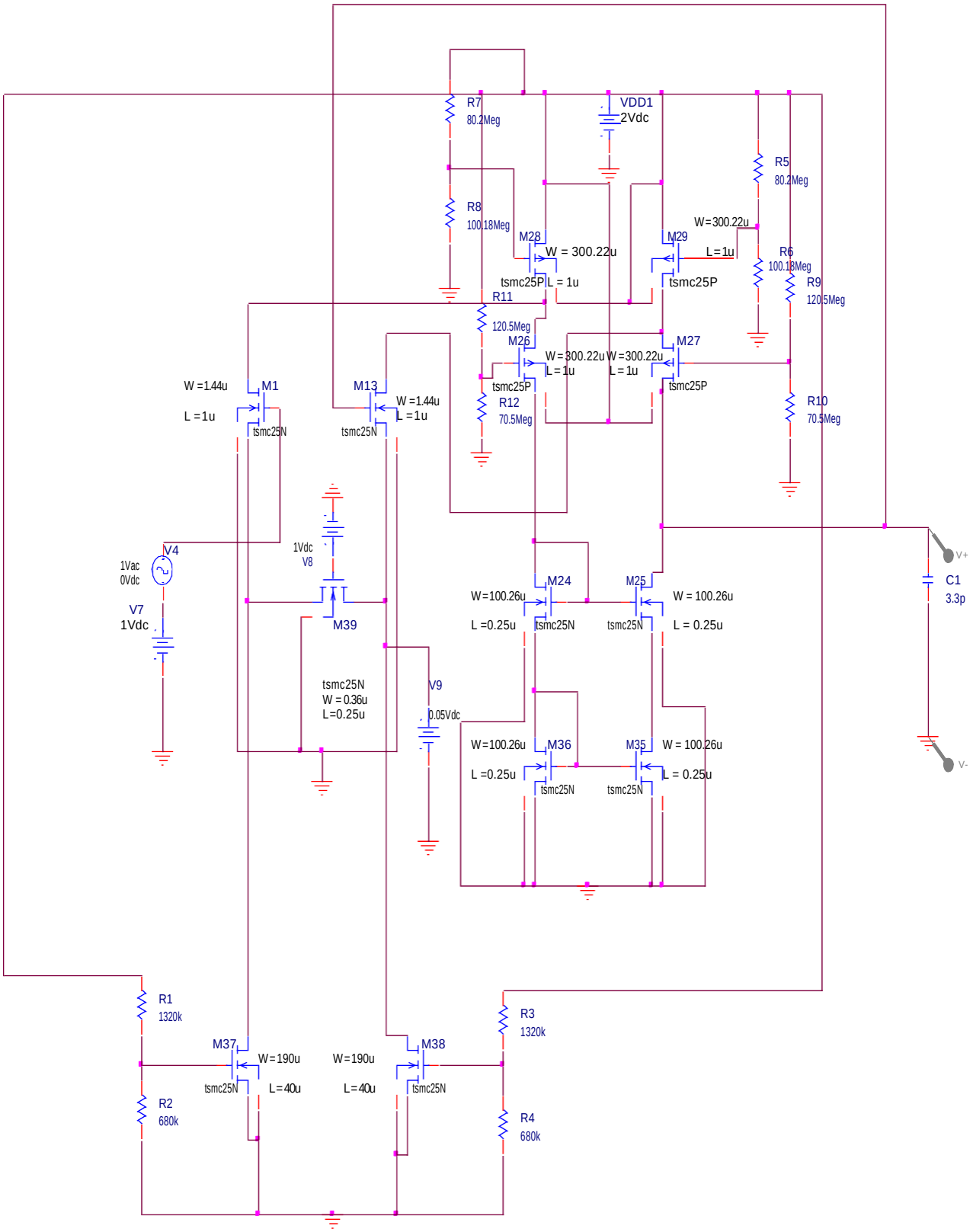
a. 4th Order low pass filter; Single-Ended VCCS (gm) Model



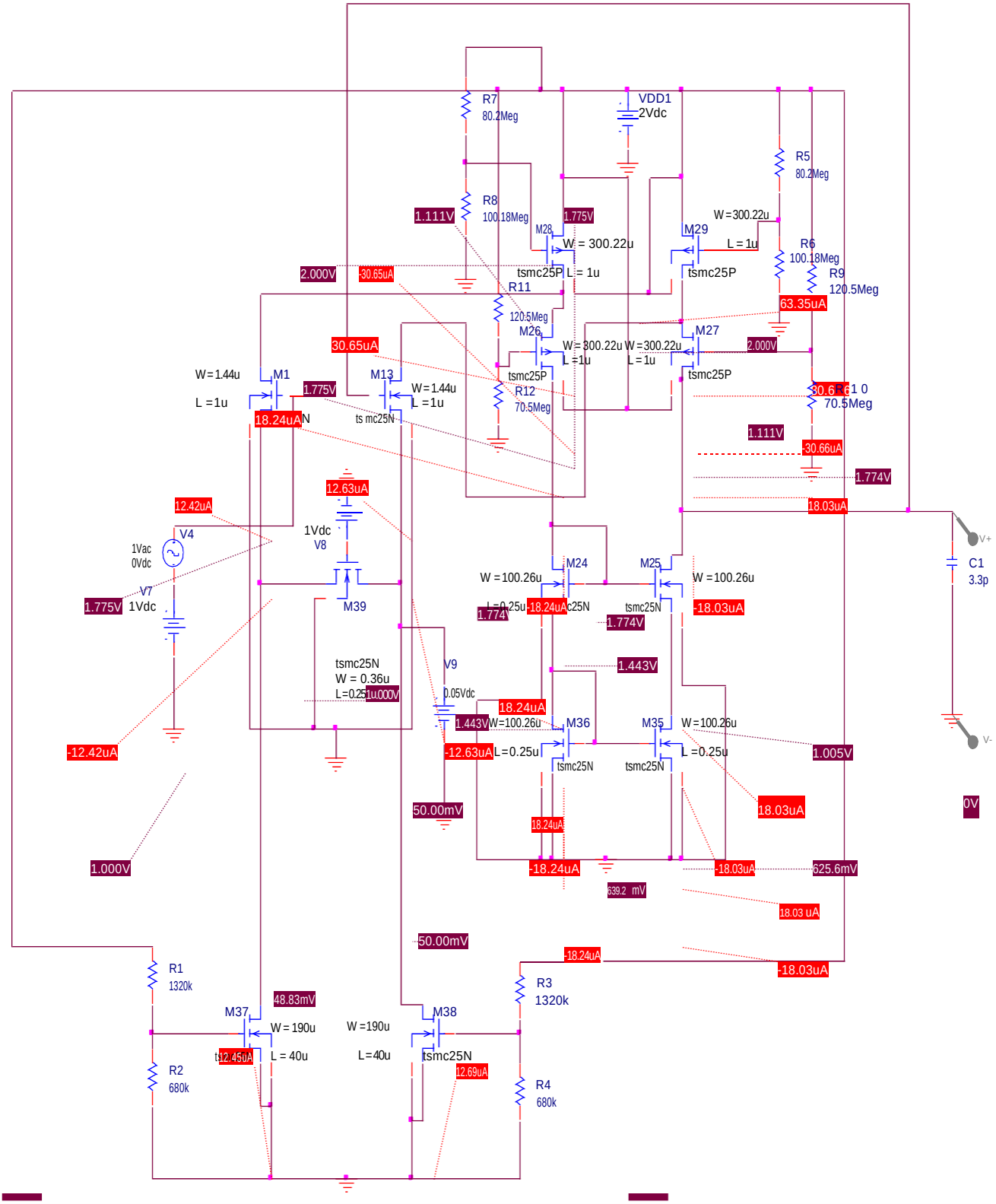
b. 4th Order low pass filter; Fully-Differential VCCS (gm) Model



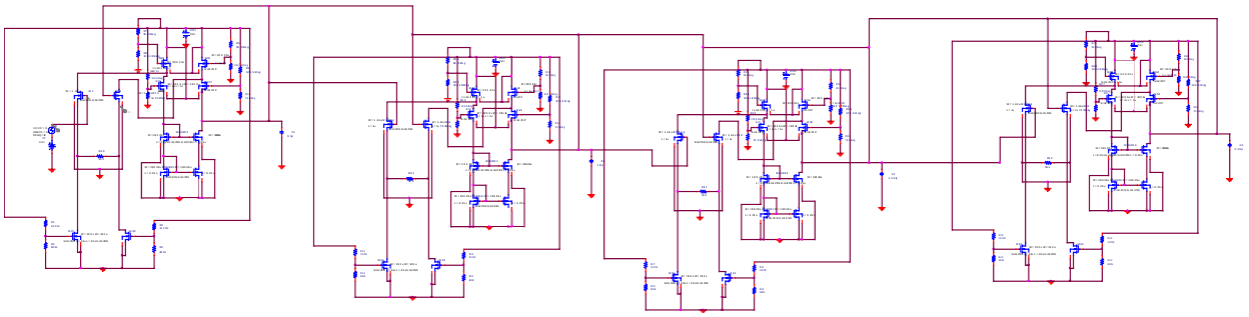
c. gm Cell model (Folded Cascode OTA) Circuit



d. SPICE Large Signal/DC Analysis of Folded Cascode OTA



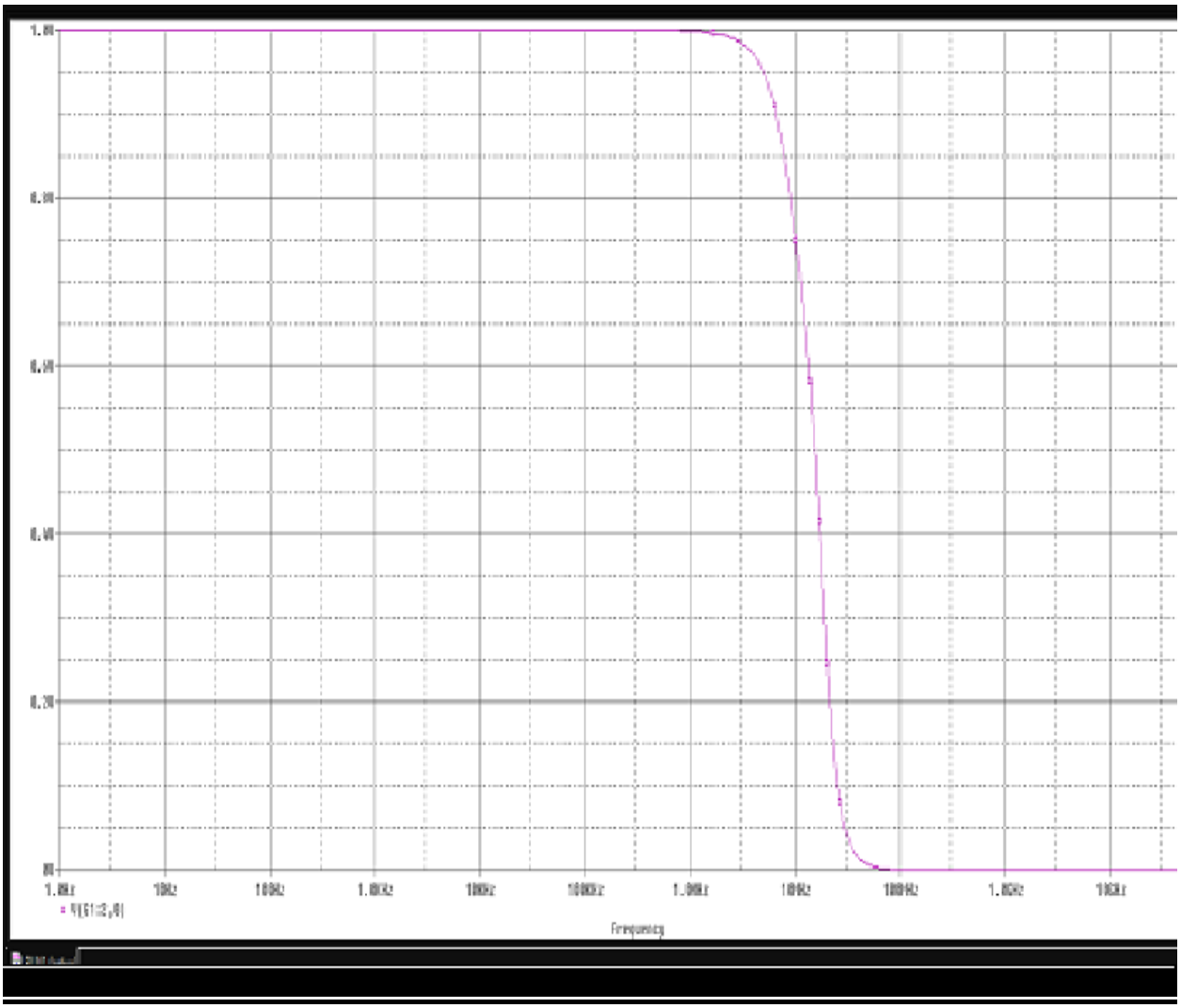
e. Final IC Design Schematic (4th Order OTA-C Filter)



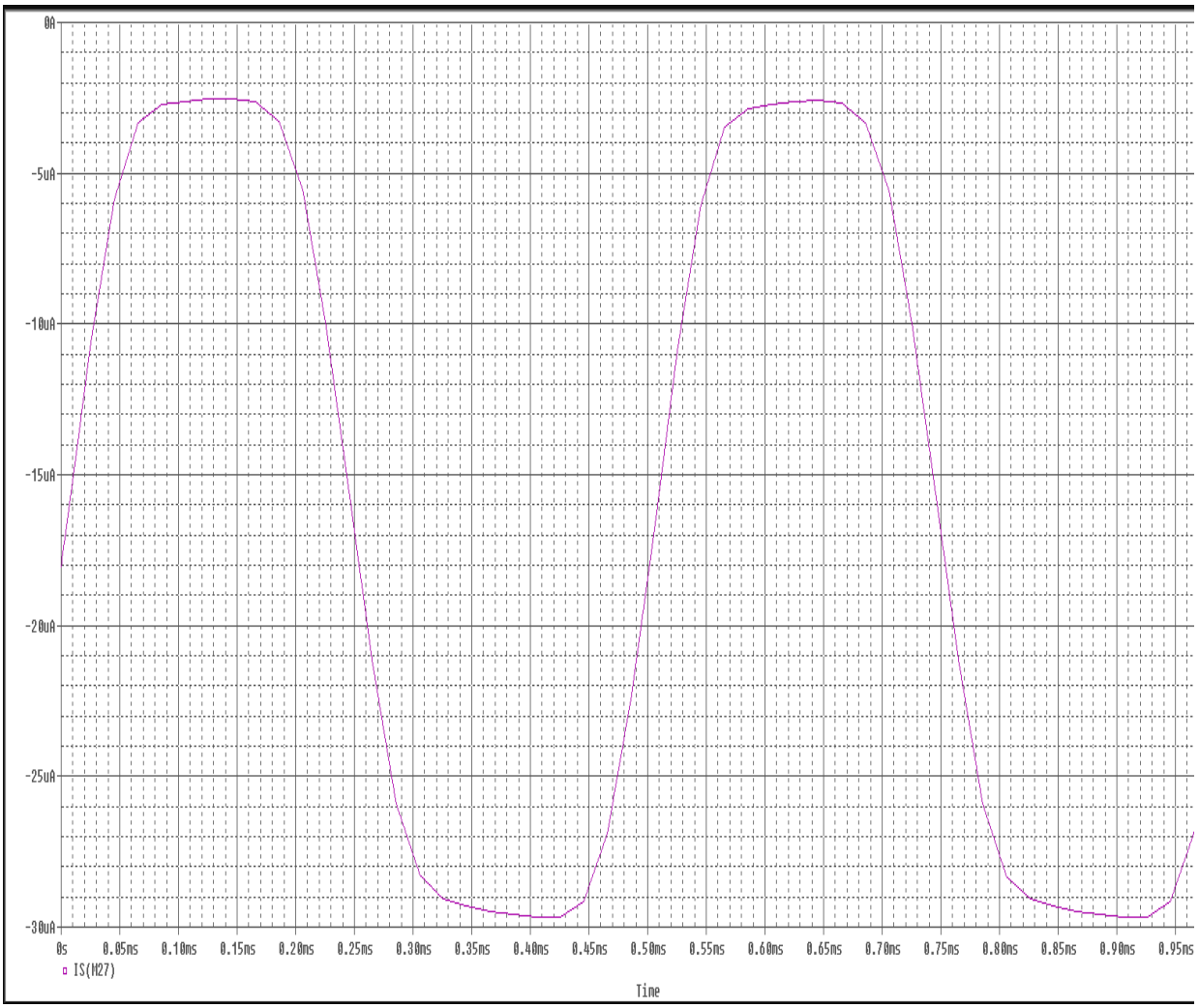
SPICE Results

Respective output SPICE Simulations

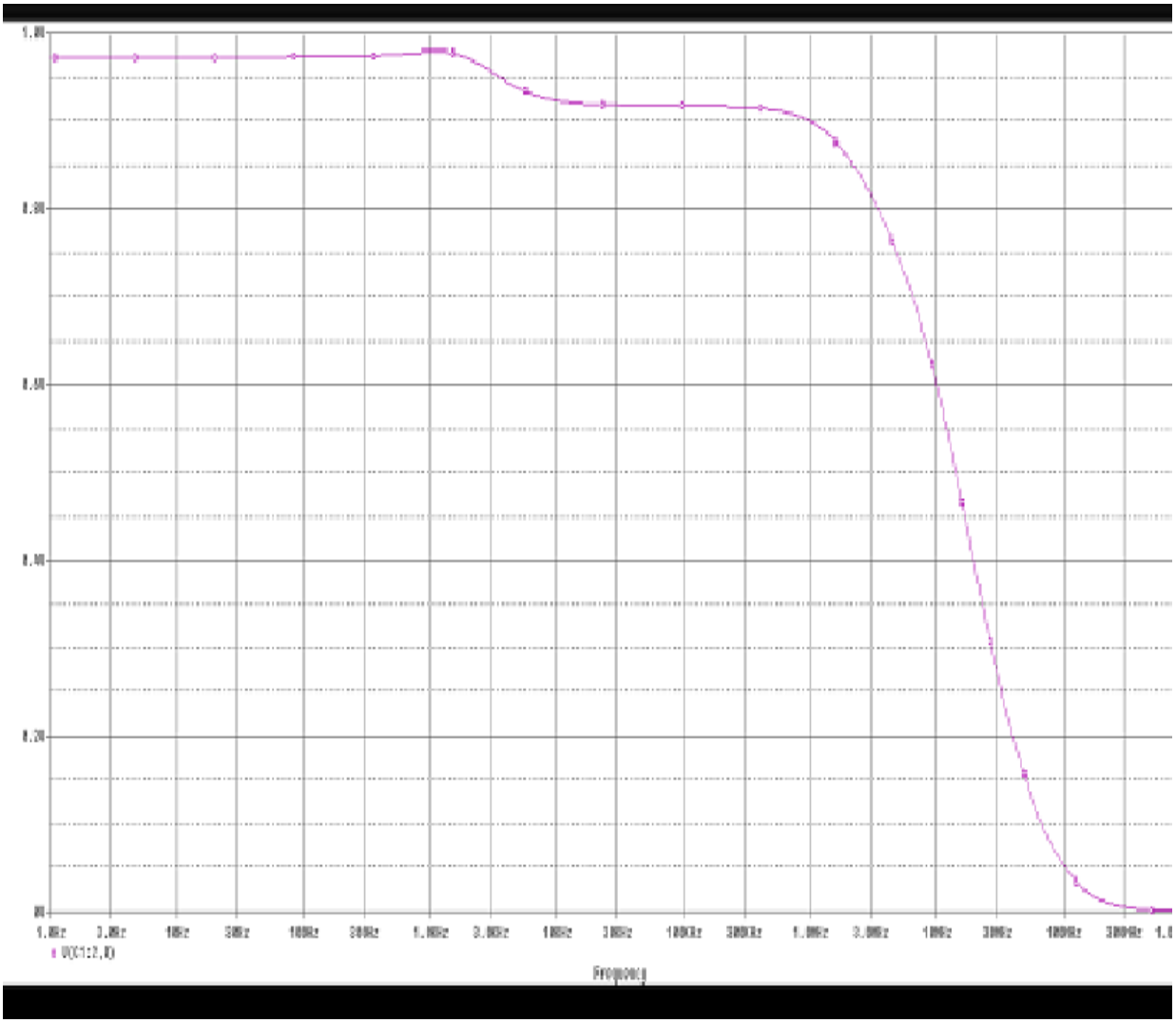
a. Ideal 4th order lowpass OTA-C Response



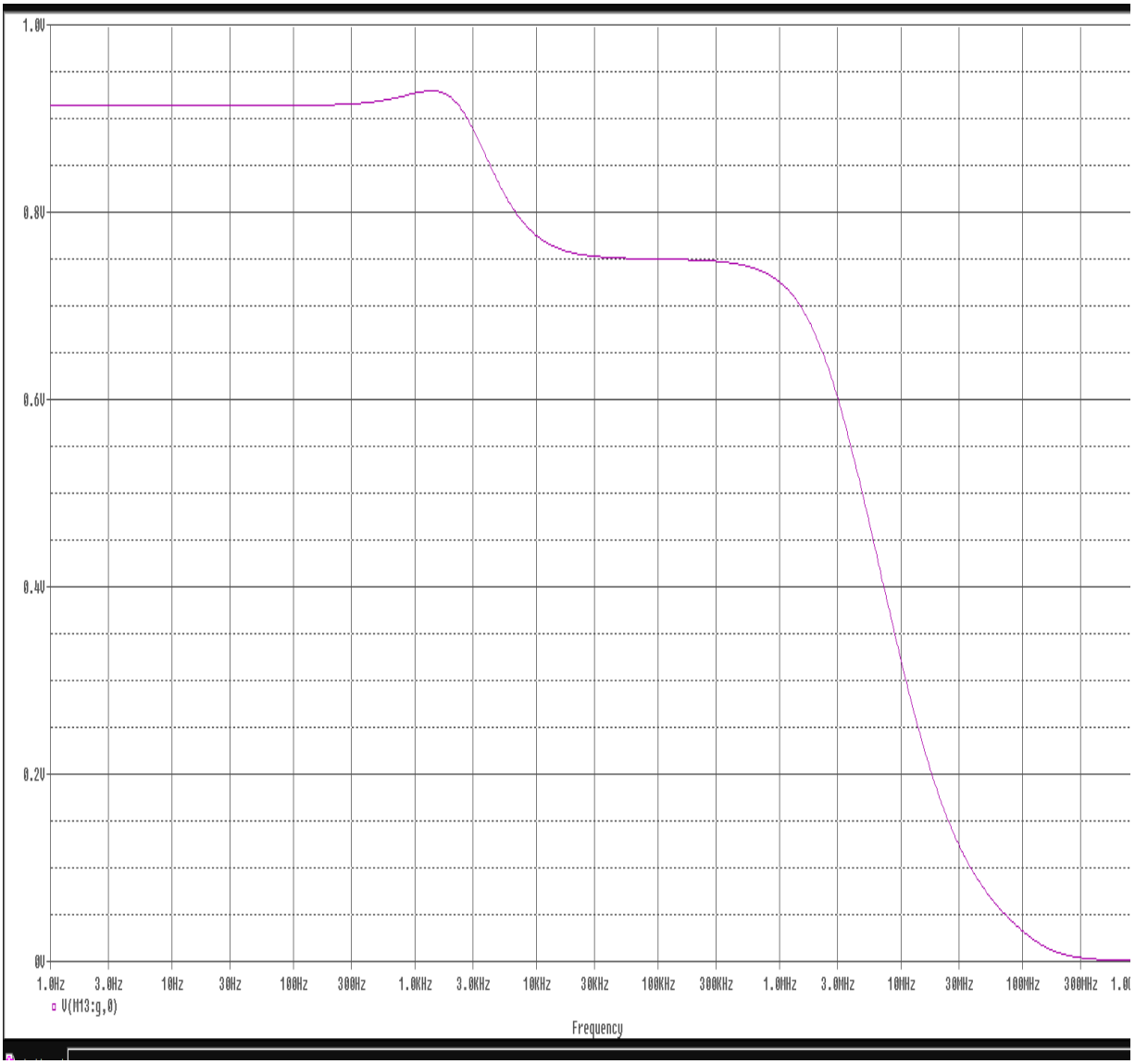
b. Transconductance Measurement for Folded-Cascode OTA block (v_{in}=1V_{pk-pk} -> g_m=i_o/v_{in}=28.6**µS**)



c. 1st Order Folded-Cascode OTA-C Response



d. 4^{th} Order OTA-C lowpass filter Response



DISCUSSION; CONCLUSION

Consequently, the OTA proved to be an essential building block in implementing continuous-time (CT) filters. This project involved several design steps which may be useful to the analog circuit designer.

In conclusion, the folded cascode OTA may be implemented using the design procedure described earlier in this paper. First stage was an NMOS implementation differential pair which was biased by a constant current source and current sink to produce equivalent current of I/2 flowing through the MOS differential transistors. The W/L ratios in the first stage were selected to be wide to handle a lot of current to produce the designed gm spec. The last stage was biasing a PMOS common gate by way of current sources and current sinks. The output current sinks W/L ratios were selected to be small in length to produce a higher output impedance.

The final design phase was testing the gm cell; since the output current spec. was not achieved, a factor of 6 was embedded in the calculations to incorporate the discrepancy. Cascading the designed OTA-C blocks, 4^{th} order lowpass implementation, resulted in more distortion at the output. Thus, challenges faced during the implementation of this project included issues getting software and hand calculations to replicate one another. Since this is rarely achievable in real-time, the compatibility rests in the designer's hands, thus, he/she must ensure proper functionality of the circuitry once implemented. For example, when replicating designed transconductance into SPICE, the measured transconductance was a factor of 6 off, and therefore as stated earlier hand calculations, and more specifically, the output capacitors had to be adjusted to incorporate this discrepancy.

As above analysis shows, the OTA is a powerful integrated tool that can be implemented in the design of CT filters if designed correctly to meet given specs, primarily linearity. Future work may concern building up on this to implement higher order filters. Challenges that may accompany that is increased power consumption and having more biasing issues from stage to stage.