ECE 532 - MICROWAVE CIRCUIT DESIGN II

144MHZ RF POWER AMPLIFIER

NAME: NASSER OSMAN

PROFESSOR: DR. CAMPBELL

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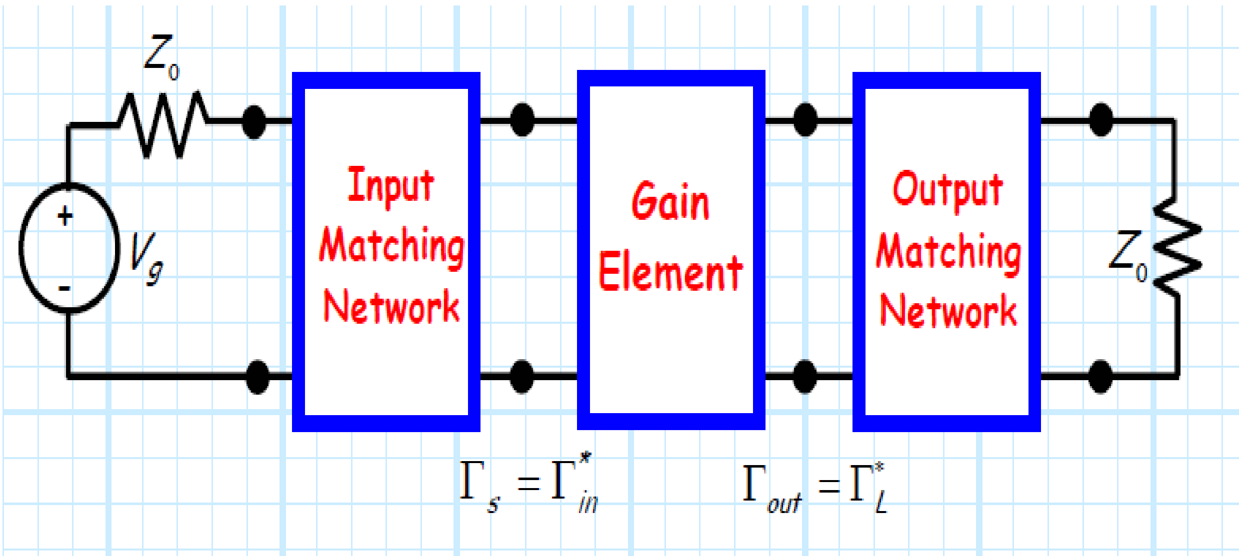
Overview; System Design Architecture

Below illustrates a two-port amplifier design terminated at 50Ω on both ends.

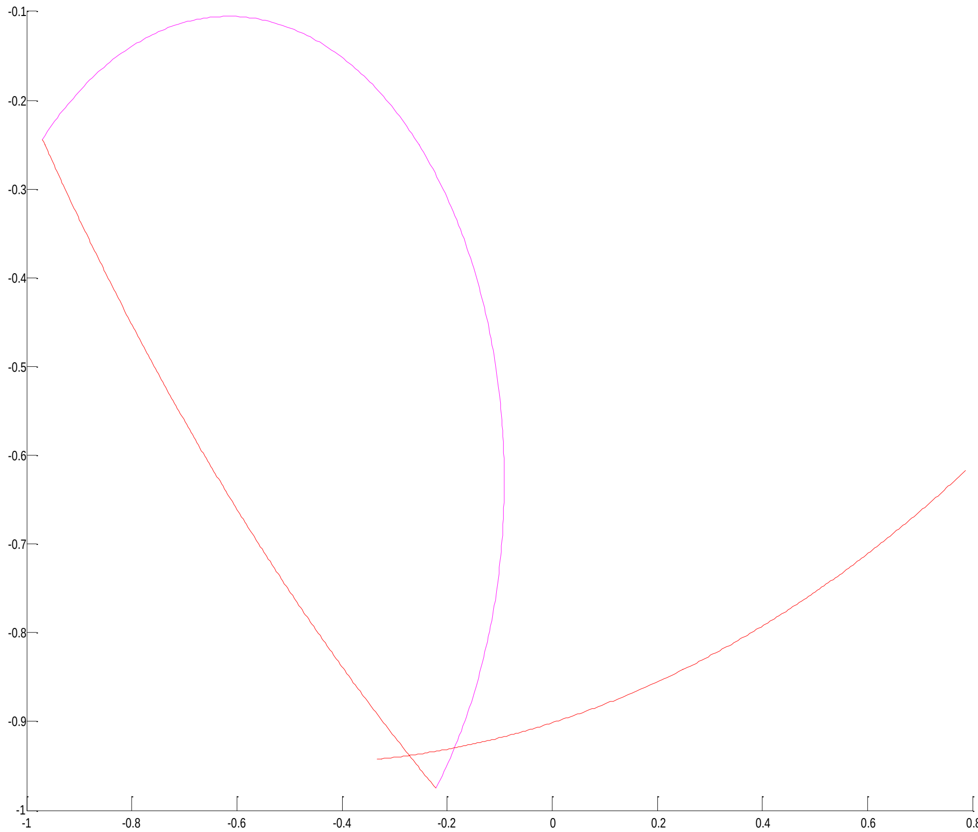


With respect to the above system design architecture, Z_0 is the 50Ω terminating characteristic impedance. Based on fundamental theory, in order to achieve maximum power gain, the amplifier's input and output port should be terminated at 50Ω. In order to realize matched impedances, a matching network must be constructed. More specifically, an input and output matching network must be designed and implemented at both the input and output port. The gain element is the amplifier.

Design Approach

The first phase of the design process involved selecting an RF transistor that would provide an acceptable gain, operating at 144MHz. A wide variety of transistors operating in the VHF band were explored. Models that were available in CAD software were given priority so as to ensure successful prototyping. Based on thorough review of S-parameter data , it was determined that NEC46134 met the design specs. whose model was also available in CAD software.

Following the selection of an RF transistor operating in the VHF band, the next phase involved analysis of the s-parameter data provided by the manufacturer, NEC. The datasheet indicated that the stability factor, k, was less than unity thus the transistor was unstable. As a result, MATLAB's RF tool was used to aid in determining an operating stable load impedance, Γ_L , and source impedance, Γ_s, by way of constructing respective input and output stability curves along with superimposed constant gain circles. The information is displayed below.

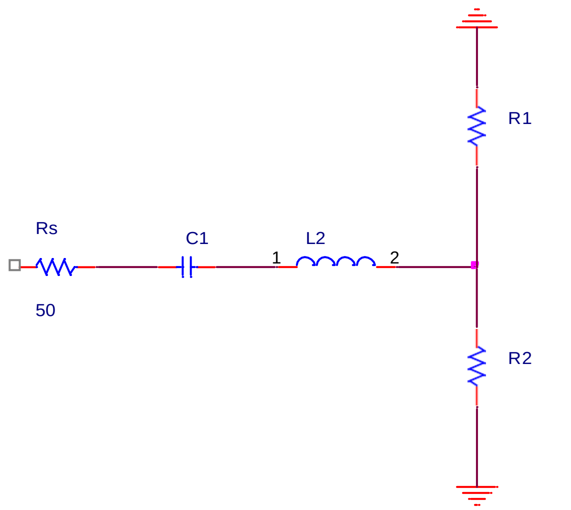


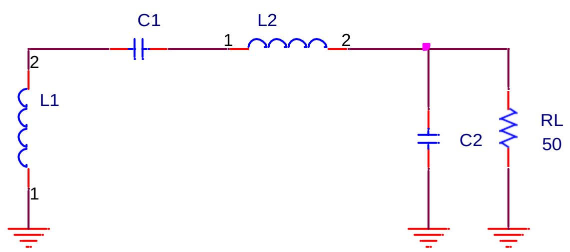
The red lines represent the stability curves (Right: Output stability curve, Left: Input stability curve) and the pink circle represents the constant 25dB constant gain circle

With respect to the above rectangular plot, it was determined that -0.33-j0.26 ($0.42\angle -142^0$) lies on the 25dB constant gain circle (highlighted in pink), thus theoretically if matched with its conjugate input impedance would provide a gain of 25dB. The source impedance, Γ_s, is calculated to be -0.146+j0.101=$0.18\angle 145.18^0$. Since both the input and output impedance reflection coefficients are located outside of the restricted operating area, they represent stable points.

Impedance Matching Network Construction

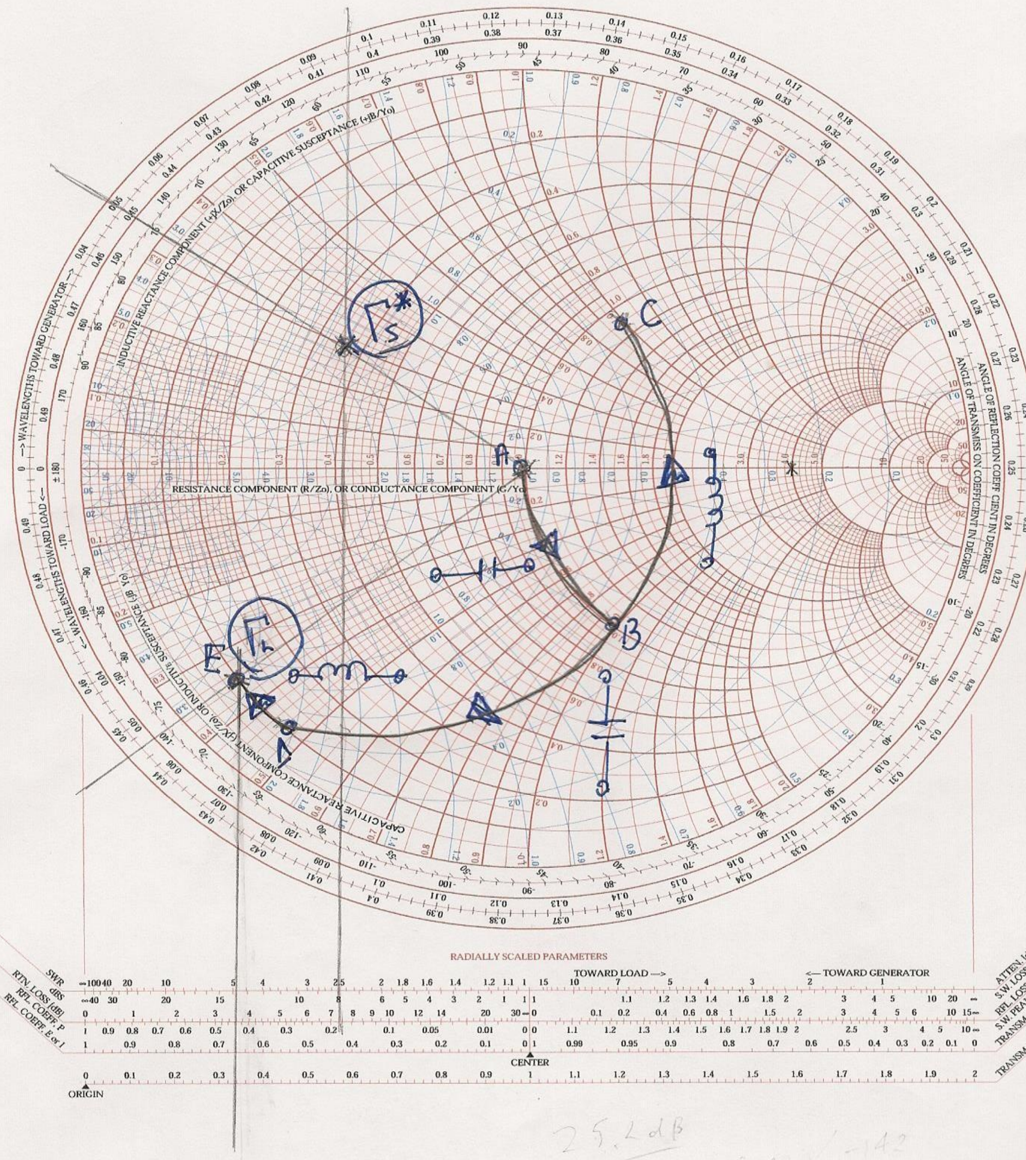
The next phase in the design process entailed constructing an appropriate impedance matching network. The impedance matching network would transform the selected transistor's input and output impedance and terminate it at 50Ω. The Smith Chart was used to aid in designing matching networks, transforming Γ_L to 50Ω and Γ_s to 50Ω. Information is shown below where RL represents the terminating load impedance and Rs is the source impedance.





NAME	TITLE ECE 532 - Project.	DWG. NO.
		DATE
SMITH CHART FORM ZY-01-N	Microwave Circuit Design - EE523 - Fall 2000	

NORMALIZED IMPEDANCE AND ADMITTANCE COORDINATES



25.2 dB

$0.42 \angle -142$

$-0.33 - j0.258$

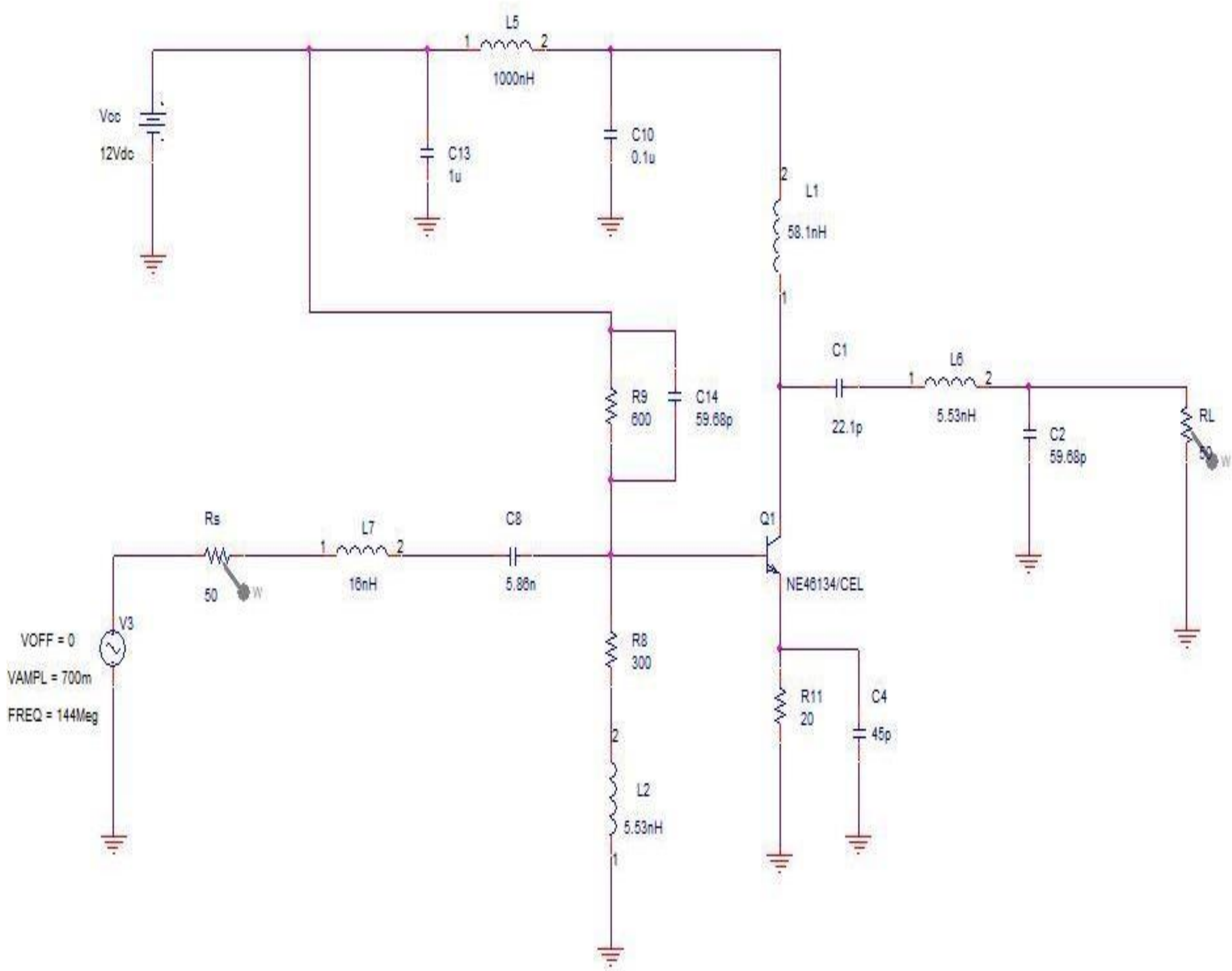
SPICE SIMULATIONS

Circuit Design Prototyping

ORCAD SPICE was the CAD software that was used to design our RF Power Amplifier.

Initial design excluded the shunt capacitor and series inductor at the biasing voltage divider at the base of the transistor. It also excluded the low pass filter at the power supply which was later constructed to eliminate high frequency noise while passing the DC power supply (Vcc).

Final Circuit Realization



Interpreted Specs.:

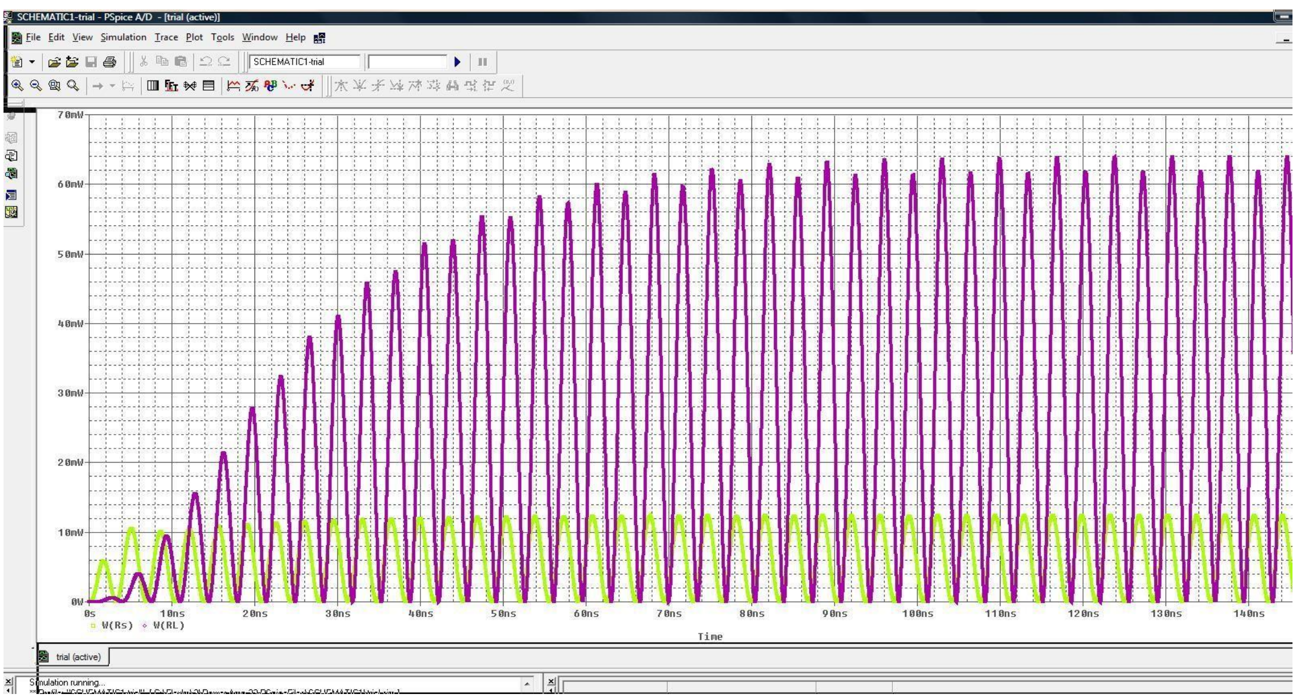
Input 700mV and 12mW Pin across 50ohm

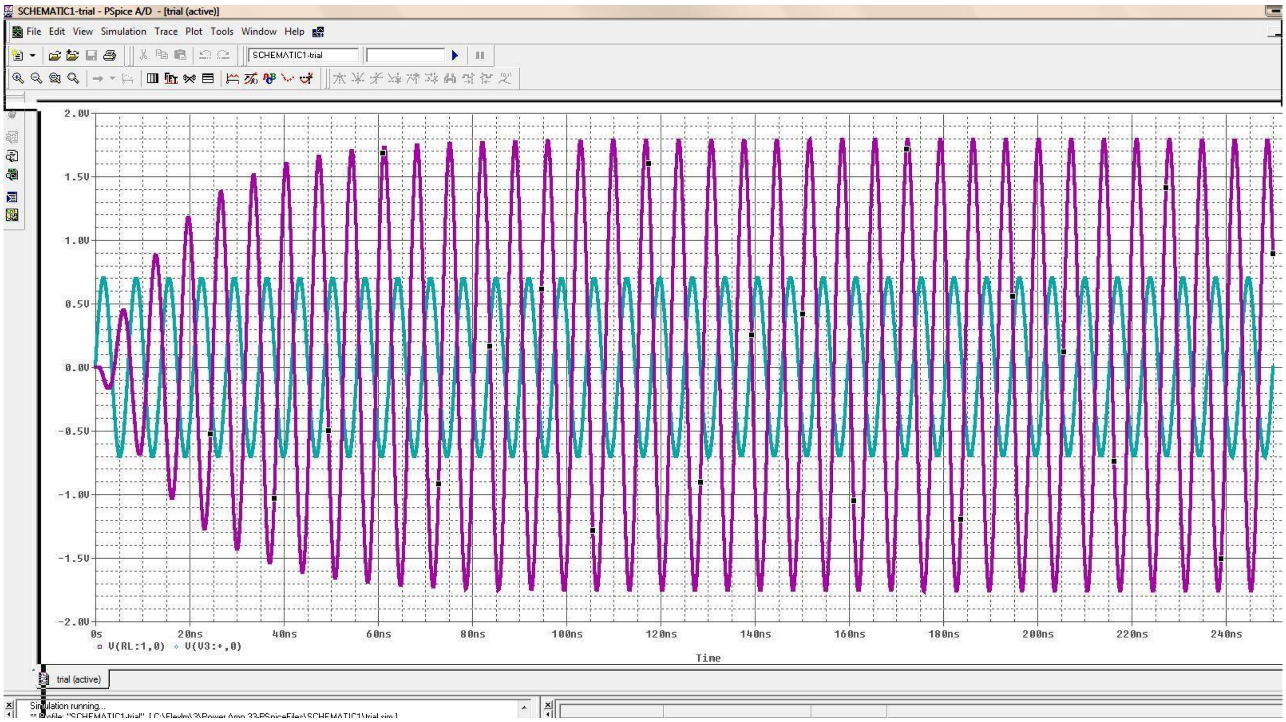
Output 1.8V and 64mW Pout across50ohm

Voltage Gain: 4.1dBm

Power Gain: 7.27dBm

(Time-domain Analysis:





Frequency Response:

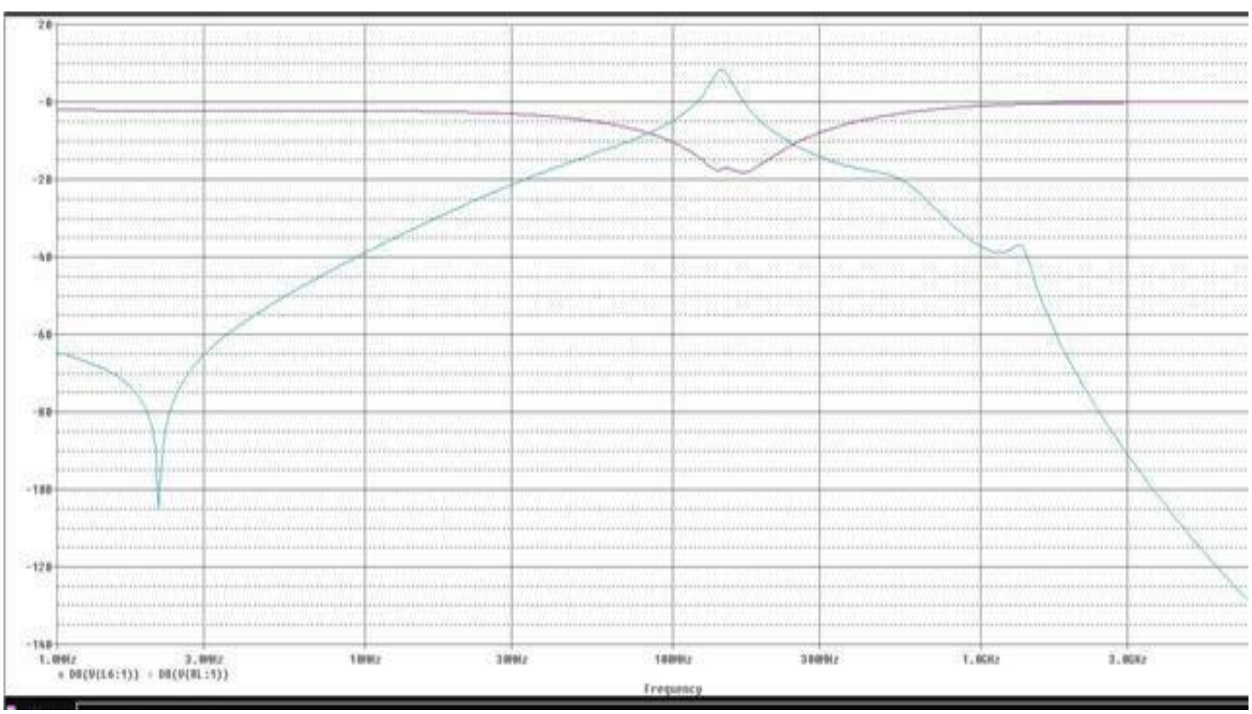


Fig2: Shows the Frequency Response of the Circuit S11 (violet), S21 (light blue)

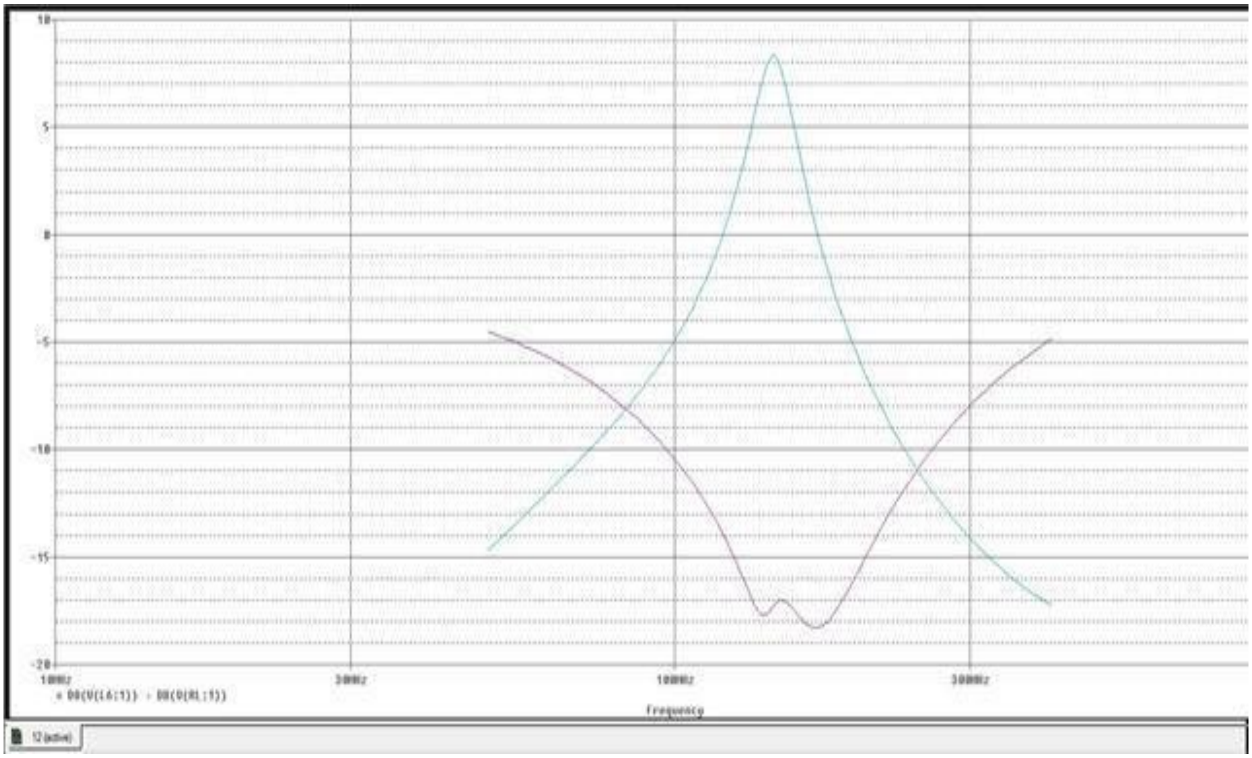


Fig3: Shows a Closer Look for the Same Frequency Response in Fig2

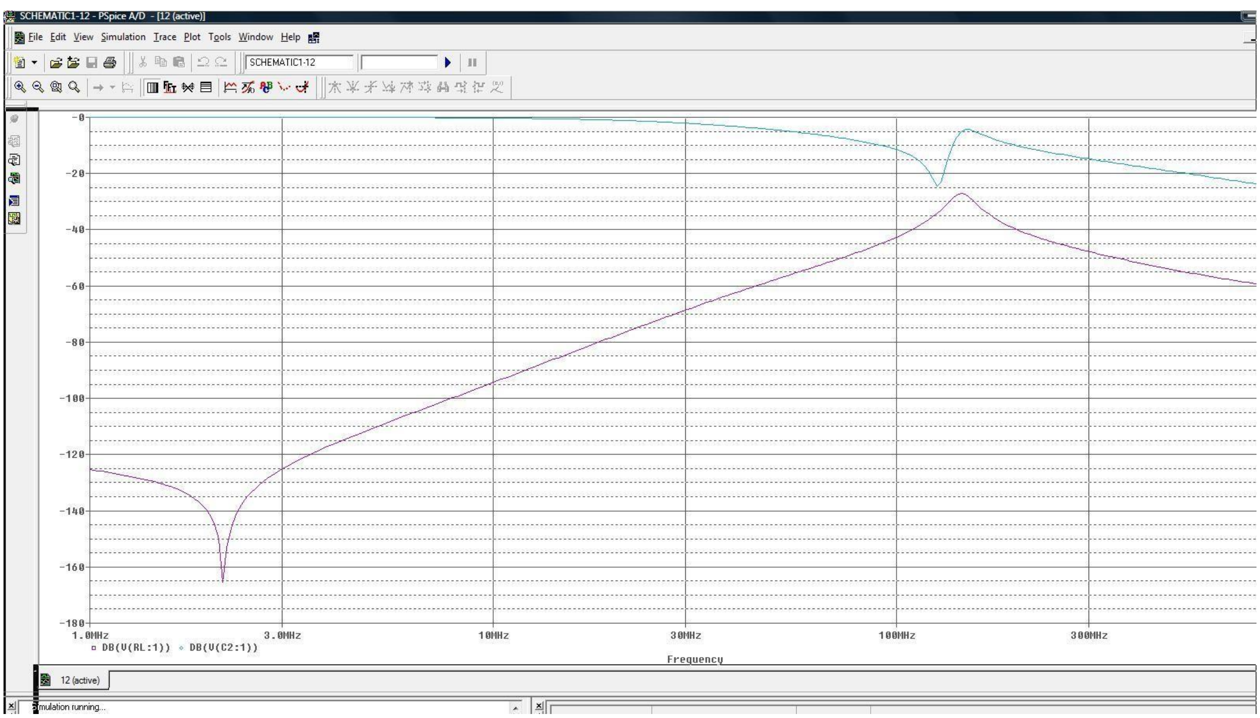
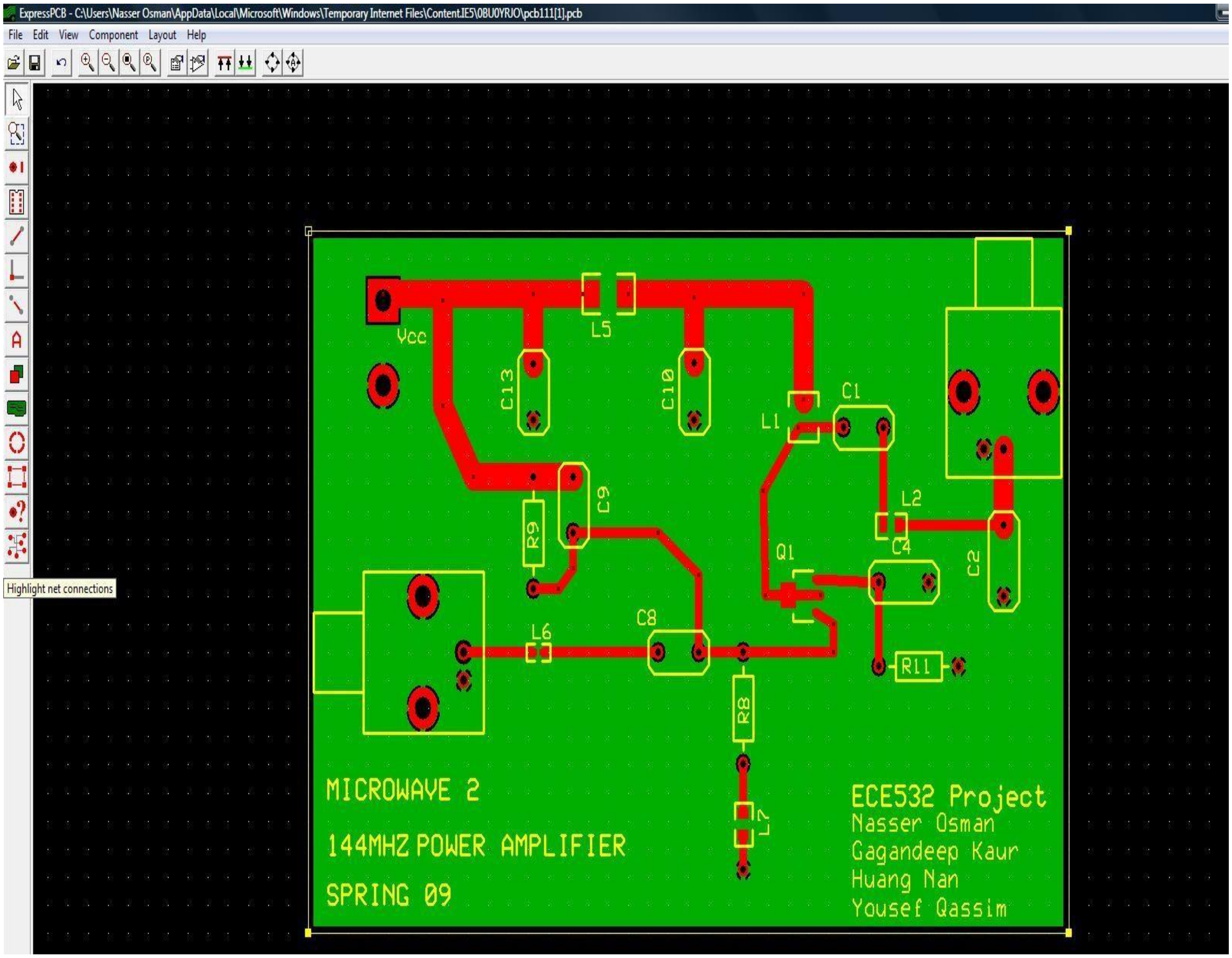
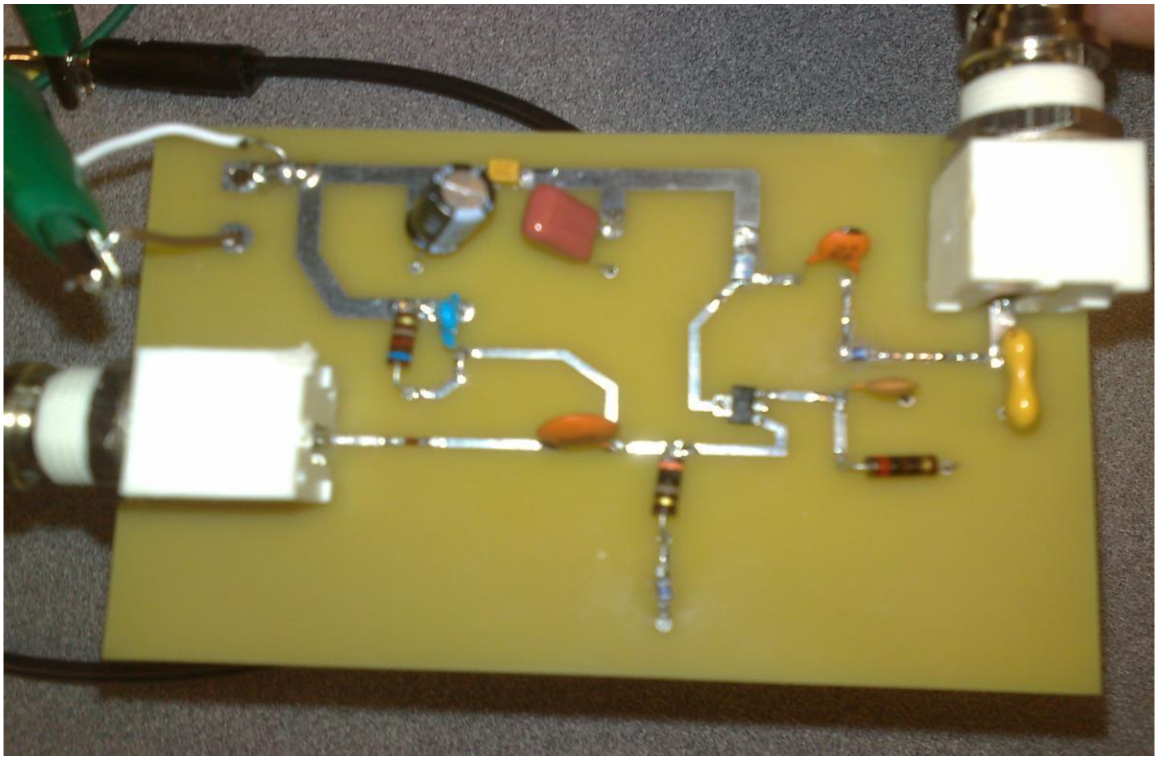


Fig4: Shows the Frequency response for S22 (light blue), and S12 (Violet)

EXPRESSPCB LAYOUT



LAB CONSTRUCTION & MEASUREMENTS



Discussion; Conclusion

The Power Amplifier project consisted of several neat activities namely CAD simulation, CAD layout using ExpressPCB software and finally the actual hardware construction. One very important note is that the project could not be fully tested because of limited access to a high frequency generation, 144MHz. Instead 100MHz was tested and was compared to that of the simulation.

What I found to be of most interest was how the project was planned into different phases and implemented, respectively. For example, CAD SPICE was used to model our hardware and proceed to the next phase which was laying it out on EXPRESSPCB. Coincidentally, if one phase encounters errors the following phase will suffer therefore each design phase had to be implemented accordingly. The hardware construction phase, too, where soldering the components onto the board (PCB) had to be given clear concentration so as to not create shorts and interruptions on the board. During the process, the transistor leads were made as short as possible on every terminal, i.e. emitter, collector, and base. Overall, I enjoyed the experience working in a team whose main objective was to get the project to work and do its job.

Group Members; Collaborations

I collaborated with fellow group members namely Yousef Qassim, Gagandeep Kaur, and Huang Nan. All were helpful and contributed in the making of the project.